1. Description

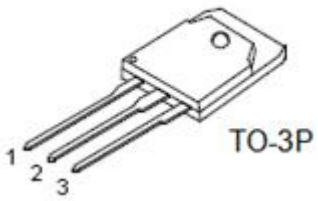
This Power MOSFET is produced using KIA advanced planar stripe DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction based on half bridge topology.

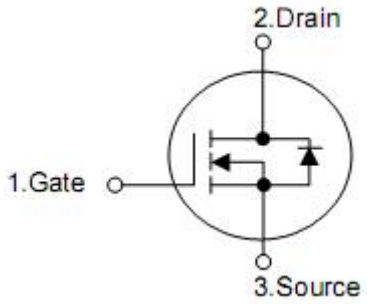
.

2. Features

- $R_{DS(on)}$=0.17Ω @ V_{GS}=10V
- Low gate charge (typical 102nC)
- Fast switching capability
- Avalanche energy specified
- Improved dv/dt capability

3. Pin configuration





Pin	Function
1	Gate
2	Drain
3	Source

4. Absolute maximum ratings

(T_C= 25 ºC , unless otherwise specified)

Parameter		Symbol	Ratings	Units
Drain-source voltage		V_{DSS}	500	V
Gate-source voltage		V_{GSS}	±30	V
Drain current continuous	T_C=25ºC	I_D	28	A
	T_C=100ºC		16.8	A
Drain current pulsed (note1)		I_{DP}	112	A
Avalanche energy	Repetitive (note1)	E_{AR}	43	mJ
	Single pulse (note2)	E_{AS}	1960	mJ
Peak diode recovery dv/dt (note 3)		dv/dt	4.5	V/ns
Total power dissipation	T_C=25ºC	P_D	479	W
	derate above 25ºC		3.83	W/ºC
Junction temperature		T_J	+150	ºC
Storage temperature		T_{STG}	-55~+150	ºC

*Drain current limited by maximum junction temperature.

5. Thermal characteristics

Parameter	Symbol	Ratings	Units
Thermal resistance,junction-ambient	R_{thJA}	62.5	ºC/W
Thermal resistance,case-to-sink typ.	R_{thCS}	0.5	
Thermal resistance,Junction-case	R_{thJC}	0.26	

6. Electrical characteristics

(T_J=25°C,unless otherwise specified)

Parameter		Symbol	Conditions	Min	Typ	Max	Units
Off characteristics							
Drain-source breakdown voltage		BV_{DSS}	V_{GS}=0V,I_D=250μA	500	-	-	V
Zero gate voltage drain current		I_{DSS}	V_{DS}=500V ,V_{GS}=0V	-	-	1	μA
			V_{DS}=400V ,T_C=125 °C	-	-	10	μA
Gate-body leakage current	Forward	I_{GSS}	V_{GS}=30V,V_{DS}=0V	-	-	100	nA
	Reverse		V_{GS}=-30V,V_{DS}=0V	-	-	-100	nA
Breakdown voltage temperature coefficient		△BV_{DSS}/△T_J	I_D=250μA	-	0.6	-	V/°C
On characteristics							
Gate threshold voltage		$V_{GS(th)}$	V_{DS}=V_{GS}, I_D=250μA	2.0	-	4.0	V
Static drain-source on-resistance		$R_{DS(on)}$	V_{DS}=10V,I_D=14A	-	0.16	0.2	Ω
Forward transconductance		g_{FS}	V_{DS}=40V,I_D=14A (note4)	-	26	-	S
Dynamic characteristics							
Input capacitance		C_{iss}	V_{DS}=25V,V_{GS}=0V, f=1MHz	-	4085	-	pF
Output capacitance		C_{oss}		-	474	-	pF
Reverse transfer capacitance		C_{rss}		-	60	-	pF
Switching characteristics							
Turn-on delay time		$t_{d(on)}$	V_{DD}=250V,I_D=28A, R_G=25Ω (note4,5)	-	45	-	ns
Rise time		t_r		-	87	-	ns
Turn-off delay time		$t_{d(off)}$		-	355	-	ns
Fall time		t_f		-	130	-	ns
Total gate charge		Q_g	V_{DS}=400V,I_D=28A , V_{GS}=10V (note4,5)	-	102	-	nC
Gate-source charge		Q_{gs}		-	43	-	nC
Gate-drain charge		Q_{gd}		-	20	-	nC
Drain-source diode characteristics							
Drain-source diode forward voltage		V_{SD}	V_{GS}=0V,I_D=28A	-	-	1.4	V
Continuous drain-source current		I_{SD}		-	-	28	A
Pulsed drain-source current		I_{SM}		-	-	112	A
Reverse recovery time		t_{rr}	I_{SD}=28A dI$_{SD}$/dt=100A/μs (note4)	-	656	-	ns
Reverse recovery charge		Q_{rr}		-	11.5	-	μC

Note:1 Repetitive rating: pulse width limited by maximum junction temperature

2. L=5mH, I_{AS}=28A,V_{DD}=50V,R_G=25Ω,staring T_J=25ºC

3. I_{SD}≤28A, di/dt≤100A/μs, V_{DD}≤BV_{DSS}, staring T_J=25 ºC

4. Pulse test: pulse width≤300μs,duty cycle≤2%

5. Essentially independent of operating temperature

7. Test circuits and waveforms

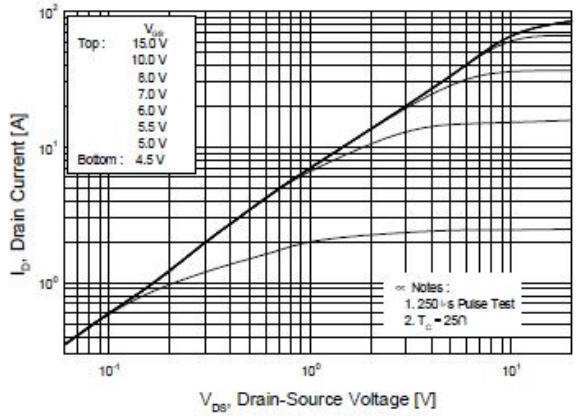


Figure 1. On-Region Characteristics

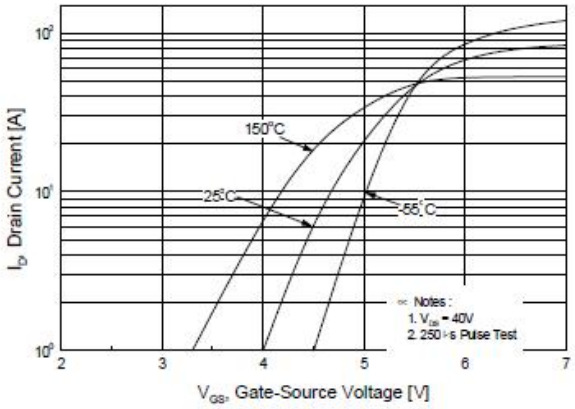


Figure 2. Transfer Characteristics

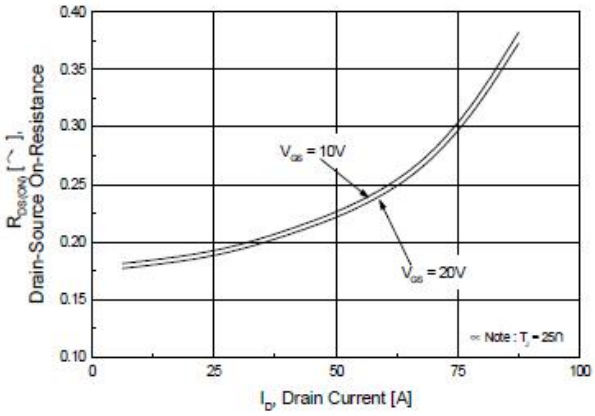


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

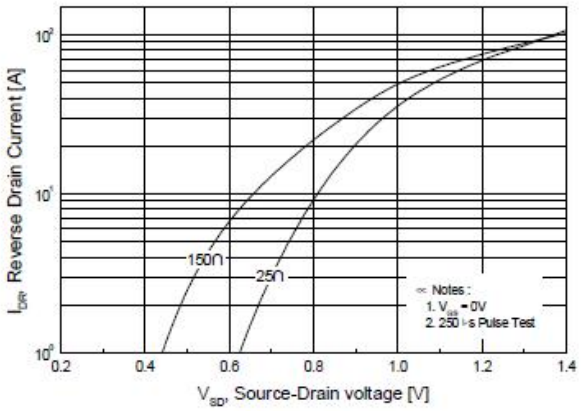


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

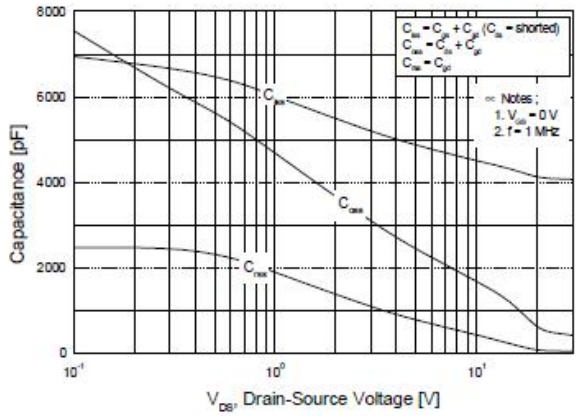


Figure 5. Capacitance Characteristics

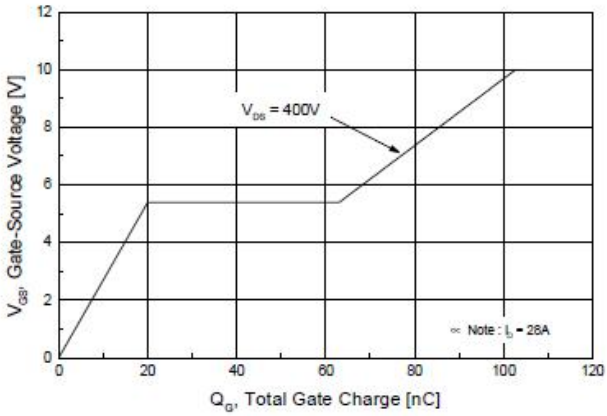


Figure 6. Gate Charge Characteristics

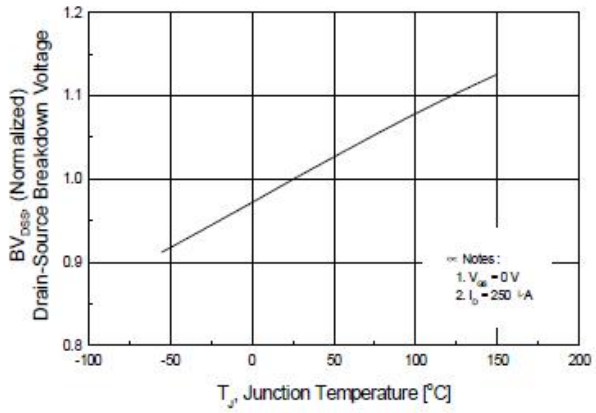


Figure 7. Breakdown Voltage Variation vs Temperature

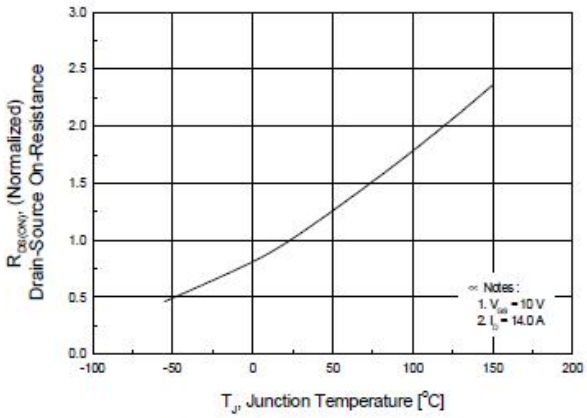


Figure 8. On-Resistance Variation vs Temperature

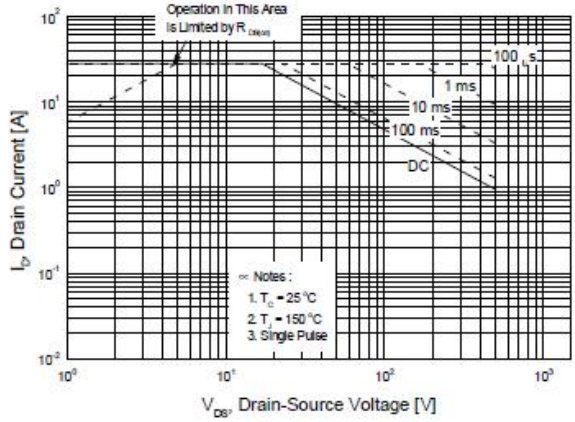


Figure 9. Maximum Safe Operating Area

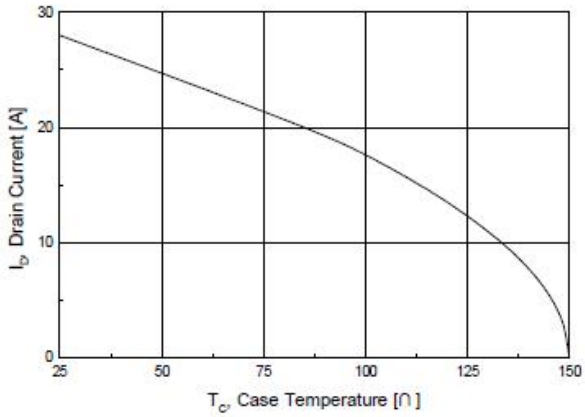


Figure 10. Maximum Drain Current vs Case Temperature

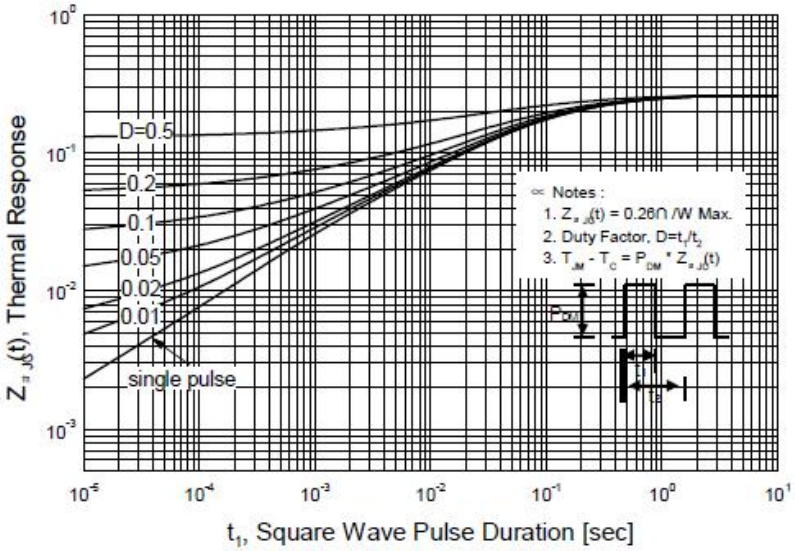


Figure 11. Transient Thermal Response Curve