

1. Features

The KIA5610 is the highest performance trench N-ch MOSFETS with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KIA5610 meet the RoHS and green product requirement, 100% EAS guaranteed with full function reliability approved.

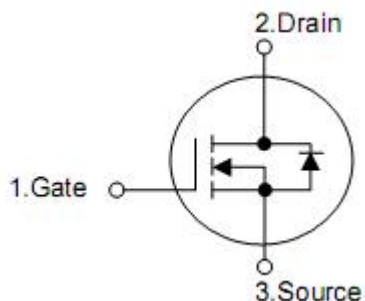
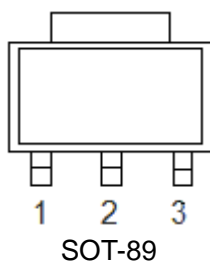
2. Features

- n $R_{DS(ON)}=98m\Omega@V_{GS}=10V$
- n Advanced high cell density trench technology
- n Super low gate charge
- n Excellent Cdv/dt effect desline
- n Green device available

3. Applications

- n High frequency point-of-load synchronous buck converter
- n Networking DC-DC power system
- n Load switch

4.Symbol



Pin	Function
1	Gate
2	Drain
3	Source

4. Absolute maximum ratings

Parameter	Symbol	Rating	Units
Drain-source voltage	V_{DSS}	100	V
Gate-source voltage	V_{GS}	± 20	V
Continuous drain current , $V_{GS}@10V$ ¹	I_D	$T_C=25^\circ C$	7*
		$T_C=100^\circ C$	5.2
		$T_A=25^\circ C$	2
		$T_A=100^\circ C$	1.4
Pulsed drain current ²	I_{DM}	14	A
Power dissipation ³	P_D	$T_C=25^\circ C$	22.7
		$T_A=25^\circ C$	2
Avalanche current	I_{AS}	6	A
Operating junction and storage temperature range	T_J, T_{STG}	-55 to 150	$^\circ C$

* Drain current limited by maximum junction temperature.

5. Thermal characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal resistance junction-case	$R_{\theta JC}$	-	2.6	$^\circ C/W$
Thermal resistance junction-ambient	$R_{\theta JA}$	-	48	

6. Electrical characteristics

(T_J=25°C, unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	100	-	-	V
BV _{DSS} temperature coefficient	ΔBV _{DSS} /ΔT _J	Reference 25°C I _D =1mA	-	0.098	-	V/°C
Drain-source on-resistance ²	R _{Ds(on)}	V _{GS} =10V, I _D =7A	-	98	115	mΩ
		V _{GS} =4.5V, I _D =5A	-	100	125	
Gate threshold voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D =250uA	1.0	1.5	2.5	V
V _{GS(TH)} temperature coefficient	ΔV _{GS(TH)}		-	-4.57	-	mV/°C
Drain-source leakage current	I _{DSS}	V _{DS} =80V, V _{GS} =0V T _J =25°C	-	-	1	μA
		V _{DS} =80V, V _{GS} =0V T _J =55°C	-	-	5	
Gate-source forward leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
Forward transconductance	g _{fs}	V _{DS} =5V, I _D =10A	-	13	-	S
Gate resistance	R _g	V _{DS} =0V, V _{GS} =0V f=1MHz	1.2	1.8	2.5	Ω
Total gate charge(10V)	Q _g	V _{DS} =80V, I _D =10A V _{GS} =10V	-	26.2	36.7	nC
Gate-source charge	Q _{gs}		-	4.6	6.44	
Gate-drain charge	Q _{gd}		-	5.1	7.1	
Turn-on delay time	t _{d(on)}	V _{DD} =50V, I _D =10A, R _G =3.3Ω, V _{GS} =10V	-	4.2	8.4	ns
Rise time	t _r		-	8.2	15	
Turn-off delay time	t _{d(off)}		-	35.6	71	
Fall time	t _f		-	9.6	19.2	
Input capacitance	C _{iss}	V _{DS} =15V, V _{GS} =0V f=1MHz	-	1535	2149	pF
Output capacitance	C _{oss}		-	60	84	
Reverse transfer capacitance	C _{rss}		-	37	52	
Continuous source current ^{1,6}	I _S	V _D =V _G =0V, Force current	-	-	7	A
Maximum pulsed current ^{2,6}	I _{SM}		-	-	14	
Diode forward voltage ²	V _{SD}	I _S =1A, V _{GS} =0V T _J =25°C	-	-	1.2	V
Reverse recovery time	t _{rr}	I _F =10A, di/dt=100A/μs T _J =25°C	-	37	-	ns
Reverse recovery charge	Q _{rr}		-	27.3	-	nC

Note:

1. The data tested by surface mounted on a 1 inch² board with 2OZ copper.
2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%.
3. The power dissipation is limited by 150 °C junction temperature.
4. The min. value is 100% EAS tested guarantee.
5. The data is theoretically the same as I_D and I_{DM}, in real applications, should be limited by total power dissipation.

7. Typical operating characteristics

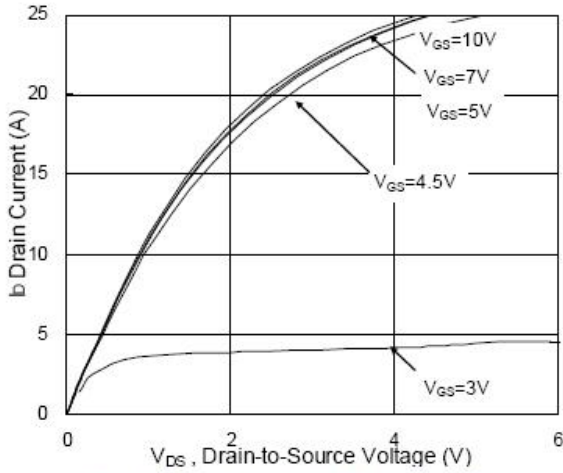


Fig.1 Typical output characteristics

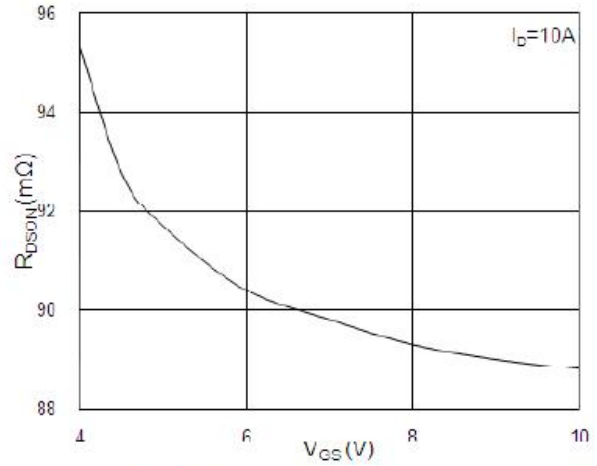


Fig.2 On-resistance vs. Gate-source

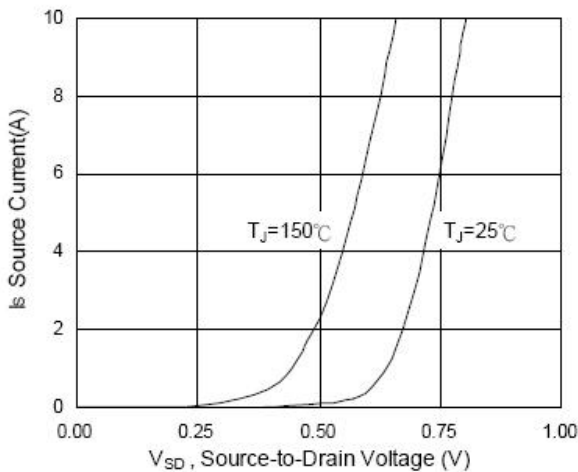


Fig.3 Forward characteristics of reverse

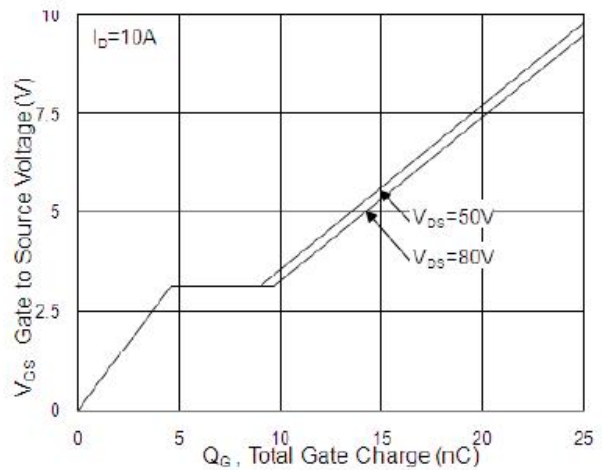


Fig.4 Gate-charge characteristics

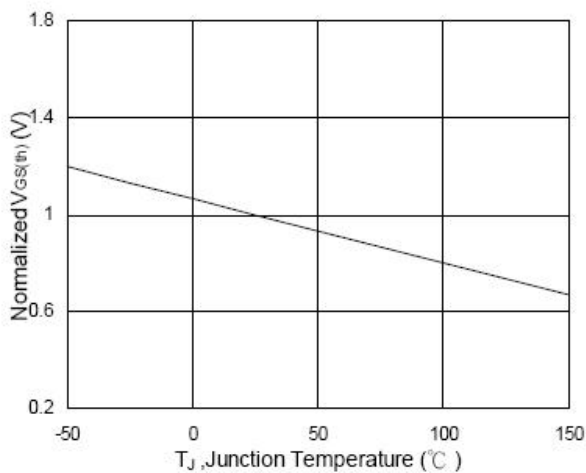


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

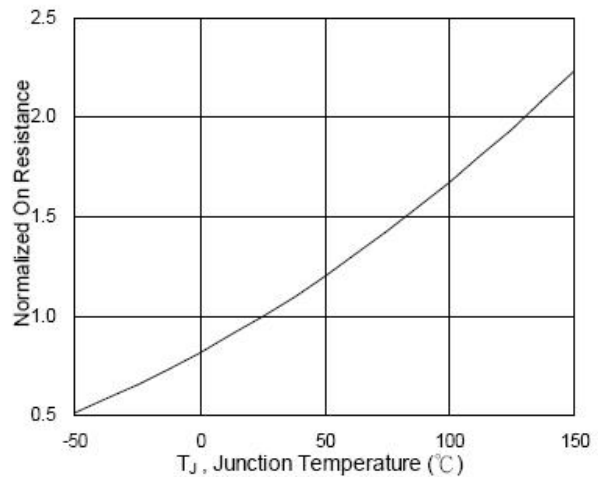


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

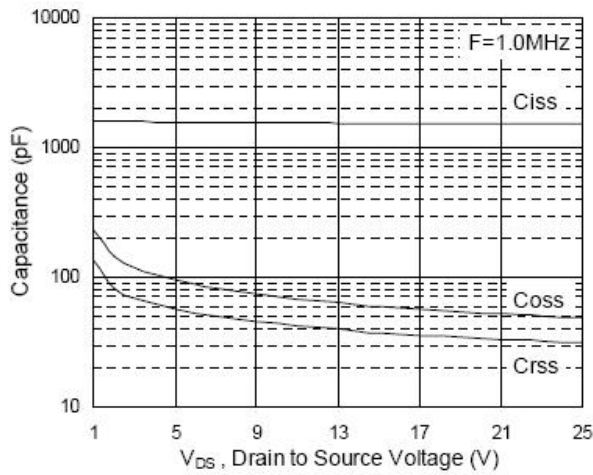


Fig.7 Capacitance

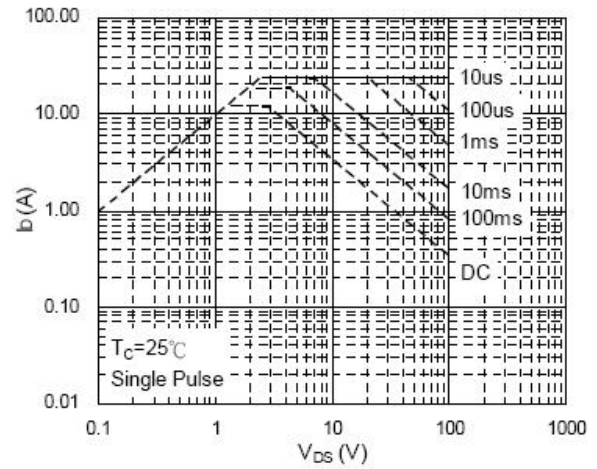


Fig.8 Safe operating area

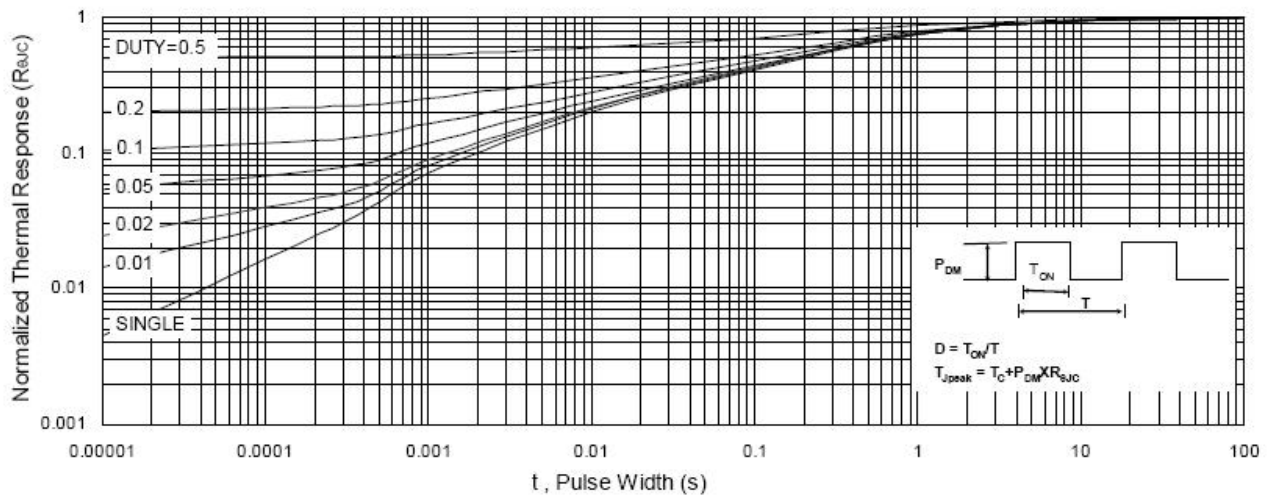


Fig.9 Normalized maximum transient thermal impedance

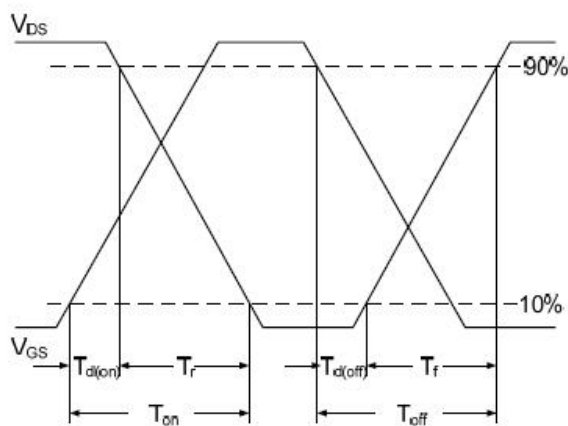


Fig.10 Switching time waveform

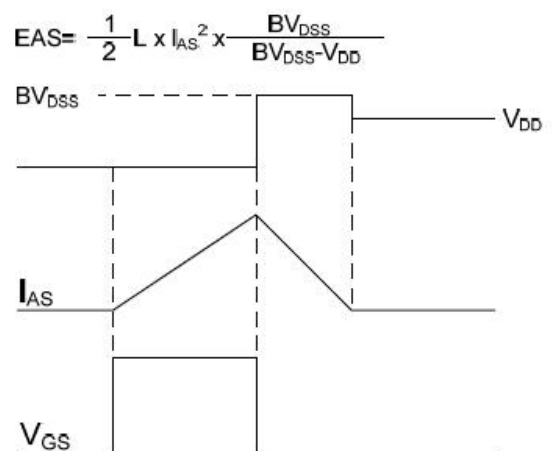


Fig.11 Gate charge waveform