

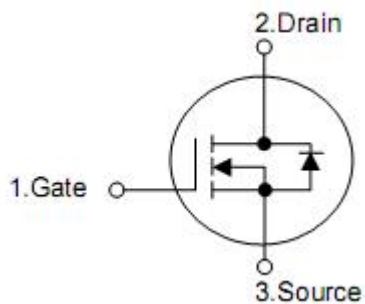
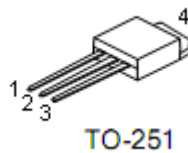
## 1. Description

The KIA8606 is the high cell density trench N-ch MOSFETS with provide excellent RDSON and gate charge for most of the synchronous buck converter applications. The KIA8606 meet the RoHS and green product requirement, 100% EAS guaranteed with full function reliability approved.

## 2. Features

- n Super low gate charge
- n 100% EAS guaranteed
- n Excellent Cdv/dt effect desline
- n Green device available
- n Advanced high cell density trench technology

## 3.Symbol



Pin	Function
1	Gate
2	Drain
3	Source
4	Drain

#### 4. Absolute maximum ratings

Parameter		Symbol	Rating	Units
Drain-source voltage		$V_{DSS}$	60	V
Gate-source voltage		$V_{GS}$	$\pm 20$	V
Continuous drain current , $V_{GS}@10V$ <sup>1</sup>	$T_C=25^\circ C$	$I_D$	35	A
	$T_C=100^\circ C$		22	
	$T_A=25^\circ C$		7.4	
	$T_A=70^\circ C$		6	
Pulsed drain current <sup>2</sup>		$I_{DM}$	80	
Power dissipation <sup>4</sup>	$T_C=25^\circ C$	$P_D$	45	W
	$T_A=100^\circ C$		2	
Single pulse avalanche energy <sup>3</sup>		$E_{AS}$	39.2	mJ
Avalanche current		$I_{AS}$	28	A
Operating junction and storage temperature range		$T_J, T_{STG}$	-55 to 150	$^\circ C$

#### 5. Thermal characteristics

Parameter	Symbol	Typ	Max	Unit
Thermal resistance junction-case <sup>1</sup>	$R_{\theta JC}$	-	2.8	$^\circ C/W$
Thermal resistance junction-ambient <sup>1</sup>	$R_{\theta JA}$	-	62	

## 6. Electrical characteristics

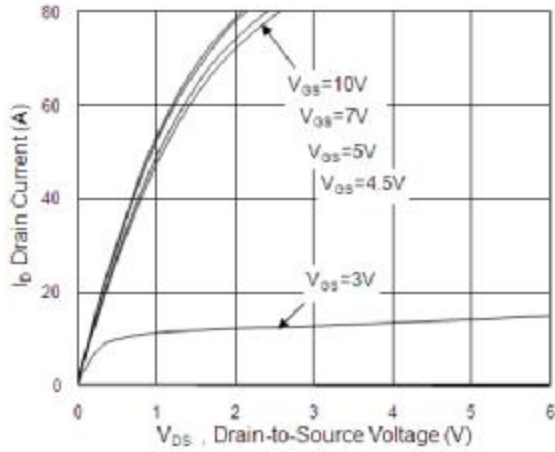
( $T_J=25^{\circ}\text{C}$ , unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	60	-	-	V
$BV_{DSS}$ temperature coefficient	$\Delta BV_{DSS}/\Delta T_J$	Reference $25^{\circ}\text{C}$ $I_D=1\text{mA}$	-	0.057	-	$\text{V}/^{\circ}\text{C}$
Drain-source on-resistance <sup>2</sup>	$R_{DS(on)}$	$V_{GS}=10V, I_D=20A$	-	-	20	m $\Omega$
		$V_{GS}=4.5V, I_D=10A$	-	-	24	
Gate threshold voltage	$V_{GS(TH)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.2	-	2.5	V
$V_{GS(TH)}$ temperature coefficient	$\Delta V_{GS(TH)}$		-	-5.68	-	$\text{mV}/^{\circ}\text{C}$
Drain-source leakage current	$I_{DSS}$	$V_{DS}=48V, V_{GS}=0V$ $T_J=25^{\circ}\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS}=48V, V_{GS}=0V$ $T_J=55^{\circ}\text{C}$	-	-	5	
Gate-source forward leakage	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
Forward transconductance	$g_{fs}$	$V_{DS}=5V, I_D=15A$	-	45	-	S
Gate resistance	$R_g$	$V_{DS}=0V, V_{GS}=0V$ $f=1\text{MHz}$	-	1.7	-	$\Omega$
Total gate charge(4.5V)	$Q_g$	$V_{DS}=48V, I_D=15A$ $V_{GS}=4.5V$	-	19.3	-	nC
Gate-source charge	$Q_{gs}$		-	7.1	-	
Gate-drain charge	$Q_{gd}$		-	7.6	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30V, I_D=15A,$ $R_G=3.3\Omega, V_{GS}=10V$	-	7.2	-	ns
Rise time	$t_r$		-	50	-	
Turn-off delay time	$t_{d(off)}$		-	36.4	-	
Fall time	$t_f$		-	7.6	-	
Input capacitance	$C_{iss}$	$V_{DS}=15V, V_{GS}=0V$ $f=1\text{MHz}$	-	2423	-	pF
Output capacitance	$C_{oss}$		-	145	-	
Reverse transfer capacitance	$C_{rss}$		-	97	-	
Continuous source current <sup>1,6</sup>	$I_S$	$V_D=V_G=0V,$ Force current	-	-	35	A
Maximum pulsed current <sup>2,6</sup>	$I_{SM}$		-	-	80	
Diode forward voltage <sup>2</sup>	$V_{SD}$	$I_S=1A, V_{GS}=0V$ $T_J=25^{\circ}\text{C}$	-	-	1	V
Reverse recovery time	$t_{rr}$	$I_F=15A, dI/dt=100A/\mu s$ $T_J=25^{\circ}\text{C}$	-	16.3	-	ns
Reverse recovery charge	$Q_{rr}$		-	11	-	nC

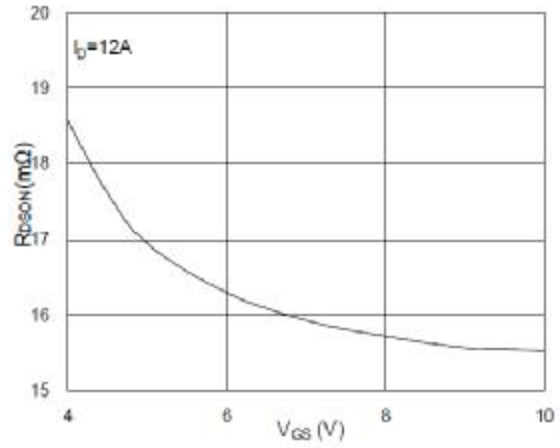
Note:

1. The data tested by surface mounted on a 1 inch<sup>2</sup> FR-4 board with 2OZ copper.
2. The data tested by pulsed, pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
3. The EAS data shows max. rating. The test condition is  $V_{DD}=25V, V_{GS}=10V, L=0.1\text{Mh}, I_{AS}=28A$
4. The power dissipation is limited by 150 °C junction temperature.
5. The data is theoretically the same as  $I_D$  and  $I_{DM}$ , in real applications, should be limited by total power dissipation.

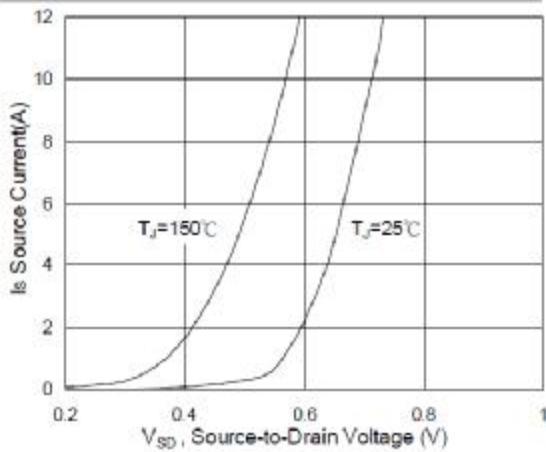
**7. Typical operating characteristics**



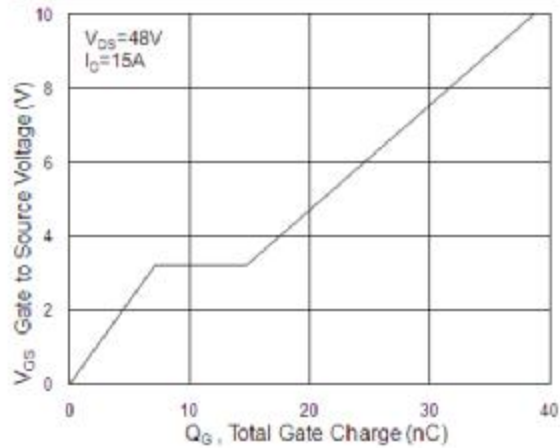
**Fig.1 Typical Output Characteristics**



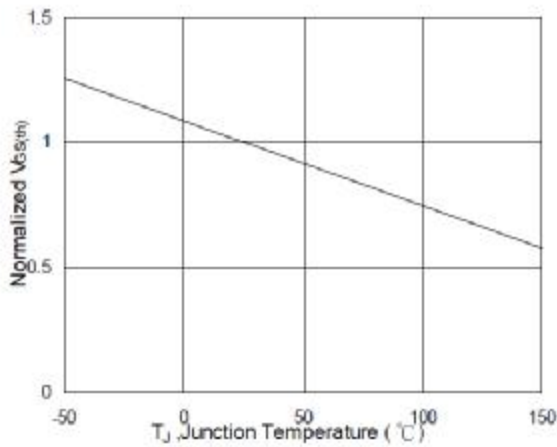
**Fig.2 On-Resistance v.s Gate-Source**



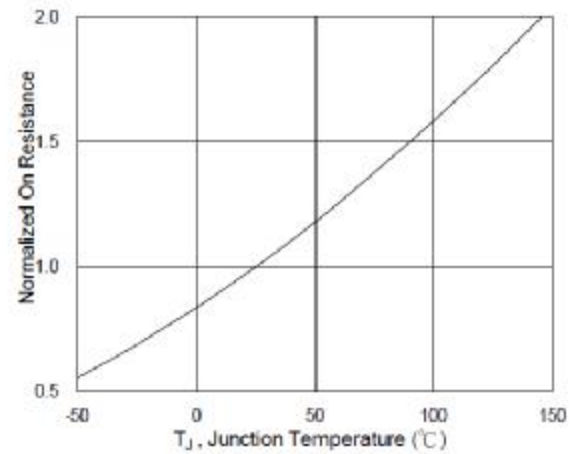
**Fig.3 Forward Characteristics of Reverse**



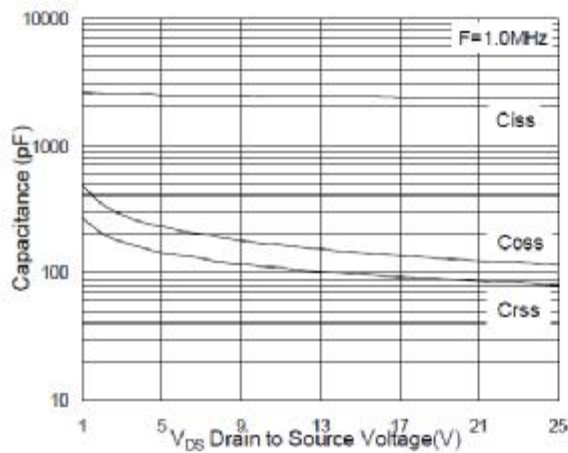
**Fig.4 Gate-Charge Characteristics**



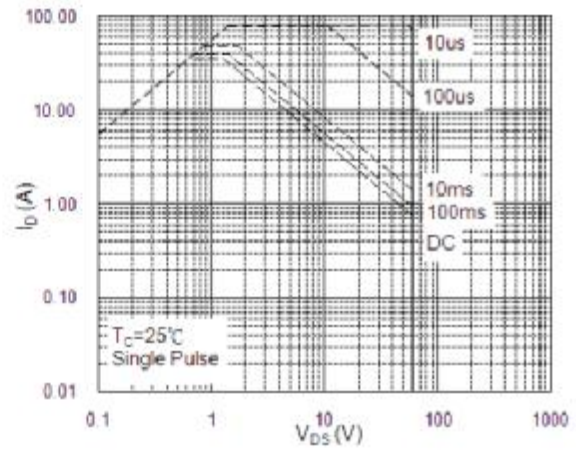
**Fig.5 Normalized  $V_{GS(th)}$  v.s  $T_J$**



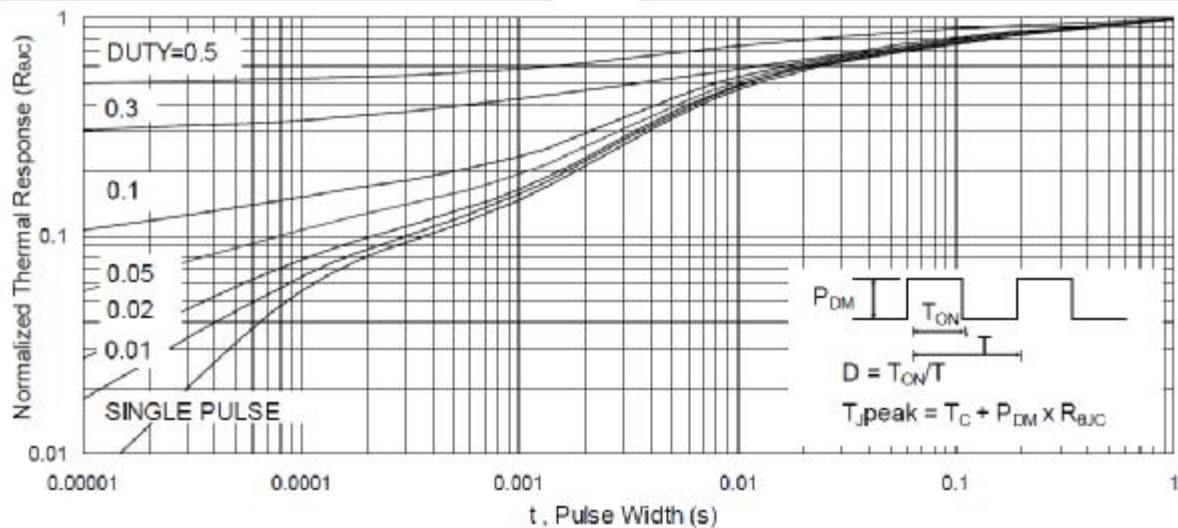
**Fig.6 Normalized  $R_{DS(on)}$  v.s  $T_J$**



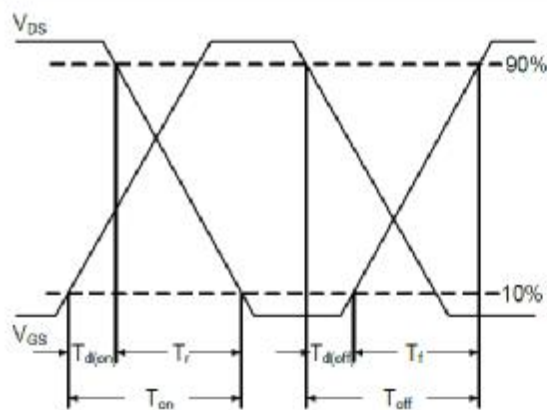
**Fig.7 Capacitance**



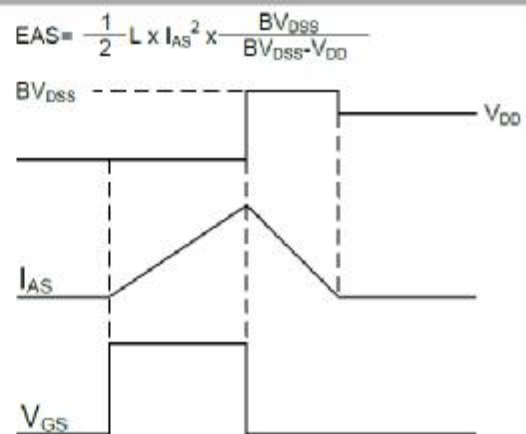
**Fig.8 Safe Operating Area**



**Fig.9 Normalized Maximum Transient Thermal Impedance**



**Fig.10 Switching Time Waveform**



**Fig.11 Unclamped Inductive Switching Waveform**