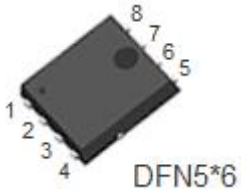
1. Features

- Proprietary New Trench Technology
- $R_{DS(ON)}$=2.2mΩ(typ.)@V_{GS}=10V
- Low Gate Charge Minimize Switching Loss
- Fast Recovery Body Diode

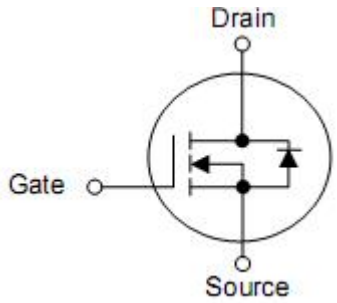
2. Applications

- High efficiency DC/DC Converters
- Synchronous Rectification
- UPS Inverter

3. Symbol



DFN5*6



Pin	Function
4	Gate
5,6,7,8	Drain
1,2,3	Source

4. Ordering Information

Part Number	Package	Brand
KNY2404A	DFN5*6	KIA

5. Absolute maximum ratings

T_C=25°C unless otherwise noted

Parameter		Symbol	Rating	Units
Drain-source voltage [1]		V_{DSS}	40	V
Gate-to-Source Voltage		V_{GSS}	±20	V
Continuous drain current [2],[3]	T_C=25°C	I_D	190	A
	T_C=100°C	I_D	108	A
Pulsed Drain Current at V_{GS}=10V [2],[4]		I_{DM}	560	A
Single pulse avalanche energy		E_{AS}	1200	mJ
Peak Diode Recovery dv/dt [3]		dv/dt	5.0	V/ns
Power dissipation		P_D	108	W
Derate above 25°C			2.0	W/°C
Maximum Temperature for Soldering Leads at 0.063in (1.6mm) from Case for 10 seconds, Package Body for 10 seconds		T_L T_{PAK}	300 260	°C
Operating junction and storage temperature range		T_J ,T_{STG}	-55 to150	ºC

Caution: Stresses greater than those listed in the ‘‘Absolute Maximum Ratings’’ may cause permanent damage to the device.

6. Thermal characteristics

Parameter	Symbol	Rating	Unit
Thermal resistance junction-case	$R_{\theta JC}$	1.15	ºC/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	75	ºC/W

7. Electrical characteristics

(T_J=25°C unless otherwise noted)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Drain-source breakdown voltage	BV_{DSS}	V_{GS}=0V,I_D=250uA	40	-	-	V
Drain-source leakage current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	uA
		V_{DS}=32V, T_C=125°C			100	
Gate-source forward leakage	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS}=10V,I_D=50A [5]	-	2.2	3.0	mΩ
Gate threshold voltage	$V_{GS(TH)}$	V_{DS}=V_{GS},I_D=250uA	2.0	-	4.0	V
Forward Transconductance	gfs	V_{DS}=10V,I_D=80A [5]	-	221	-	S
Gate Series Resistance	R_G	f=1MHz	-	2.1	-	Ω
Input capacitance	C_{iss}	V_{DS}=25V,V_{GS}=0V f=1MHz	-	4.82	-	pF
Reverse transfer capacitance	C_{rss}		-	0.41	-	pF
Output capacitance	C_{oss}		-	0.66	-	pF
Total gate charge	Q_g	V_{DD}=20V, I_D=80A V_{GS}=0~10V	-	94	-	nC
Gate-source charge	Q_{gs}		-	26	-	nC
Gate-drain charge	Q_{gd}		-	27	-	nC
Turn-on delay time	$t_{d(on)}$	V_{DD}=20V,V_{GS}=10V, R_G=2.5Ω, I_D=80A		20		ns
Rise time	t_r			23		ns
Turn-off delay time	$t_{d(off)}$			54		ns
Fall time	t_f			20		ns
Continuous Source Current [2]	I_{SD}	Integral PN-diode in MOSFET			140	A
Pulsed Source Current[2]	I_{SM}		-	-	560	
Diode forward voltage	V_{SD}	I_S=80A,V_{GS}=0V,	-	0.9	1.5	V
Reverse Recovery Time	t_{rr}	V_{GS}=0V,I_F=80A, dI_F/dt=100A/μs [4]	-	46	-	nS
Reverse Recovery Charge	Q_{rr}		-	19	-	nC

Note:
1) T_J=+25 ºC to +150 ºC
2) Silicon limited current only.
3) Package limited current.
4) Repetitive rating; pulse width limited by maximum junction temperature.
5) Pulse width≤380us; duty cycle≤2%.

8. Typical operating characteristics

Figure 1. Maximum Effective Thermal Impedance, Junction-to-Case

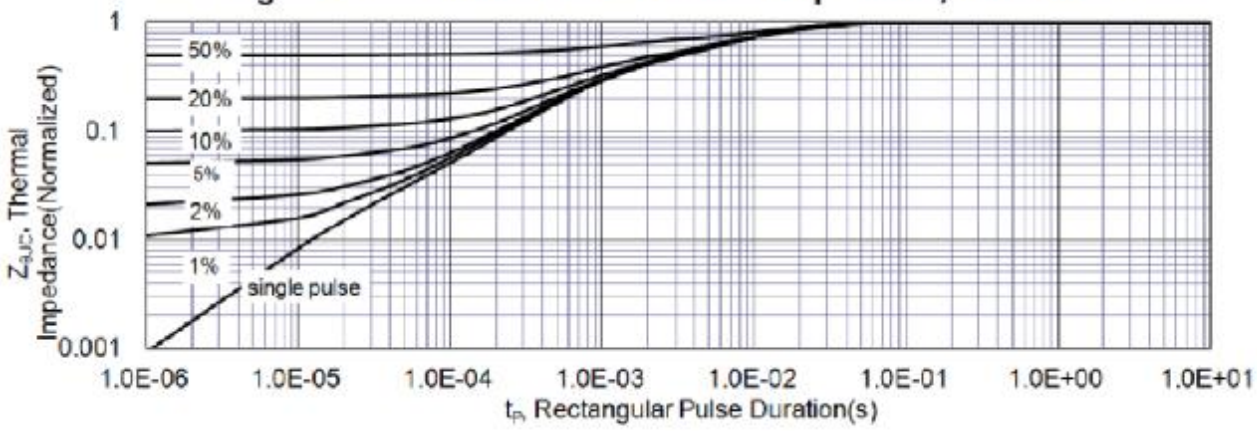


Figure 2. Maximum Power Dissipation vs Case Temperature

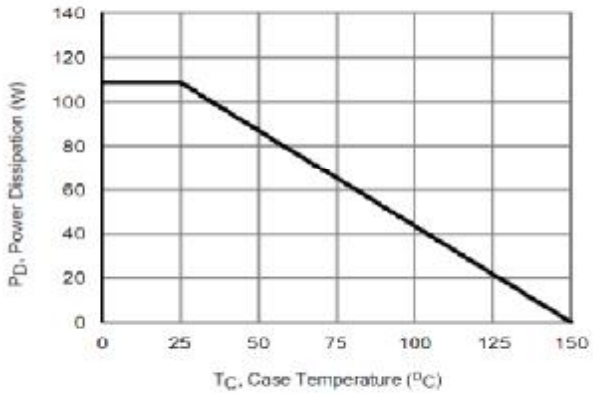


Figure3. Maximum Continuous Drain Current vs Case Temperature

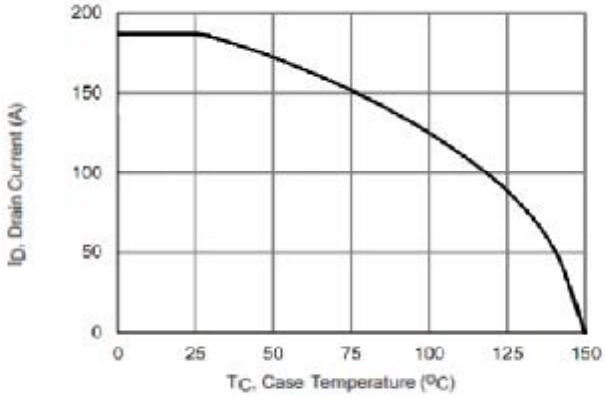


Figure 4. Typical Output Characteristics

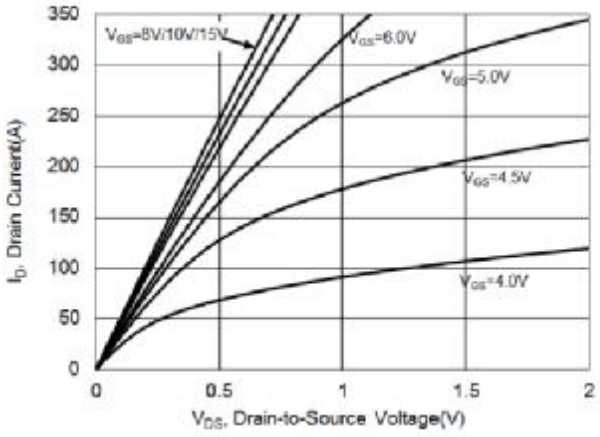


Figure 5. Typical Drain-to-Source ON Resistance vs. Gate Voltage

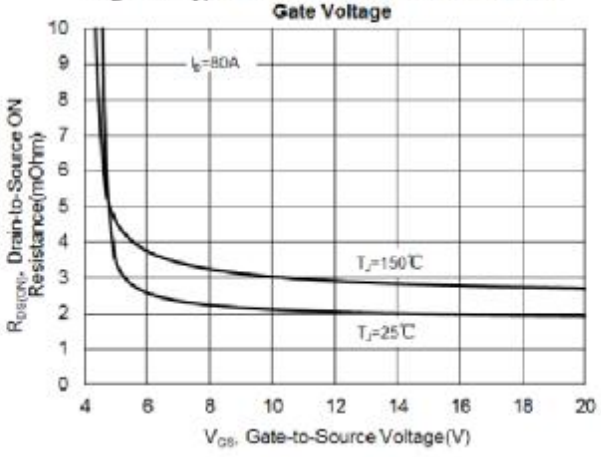


Figure 6. Maximum Peak Current Capability

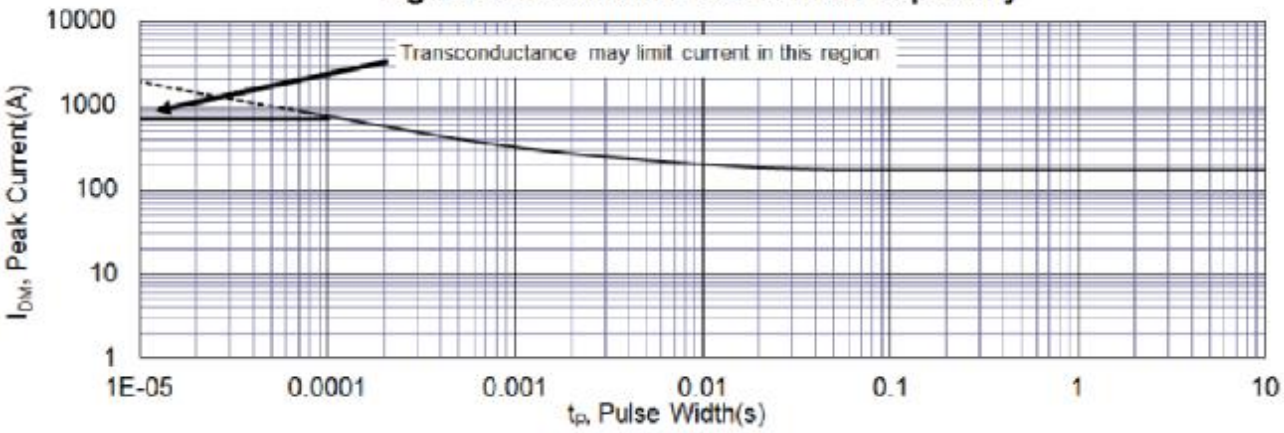


Figure 7. Typical Transfer Characteristics

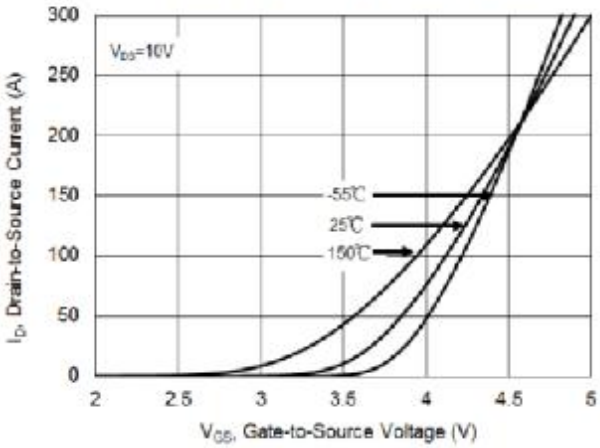


Figure 8. Unclamped Inductive Switching Capability

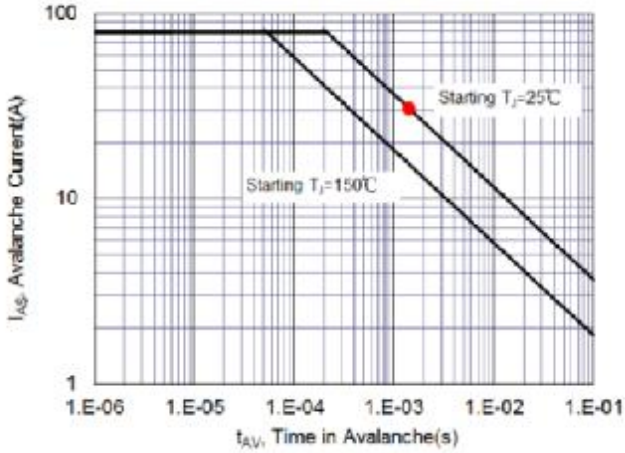


Figure 9. Typical Drain-to-Source ON Resistance

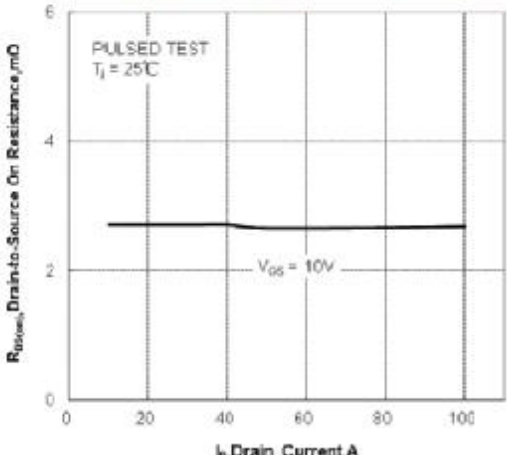


Figure 10. Typical Drain-to-Source On Resistance vs. Junction Temperature

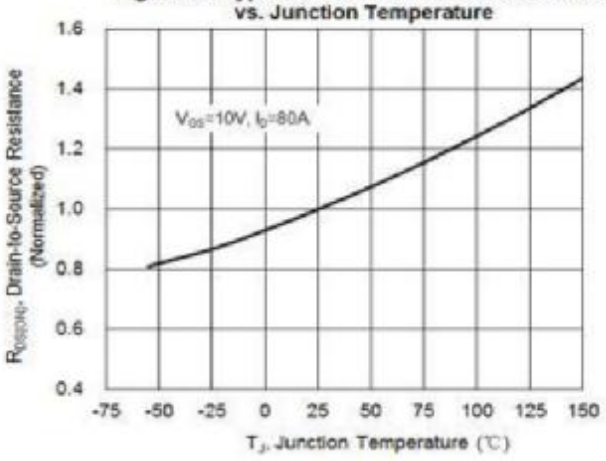


Figure 11. Typical Breakdown Voltage vs. Junction Temperature

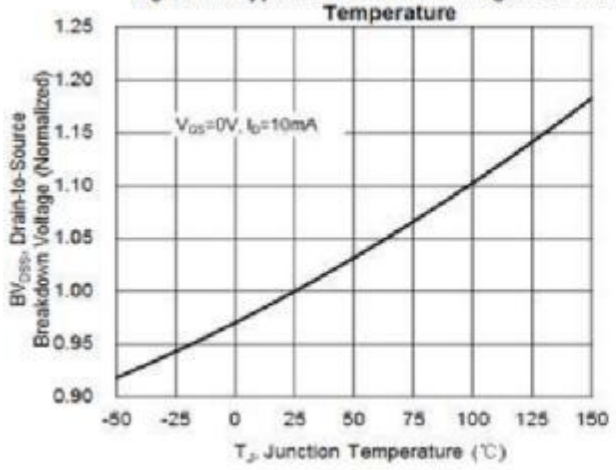


Figure 12. Typical Threshold Voltage vs. Junction Temperature

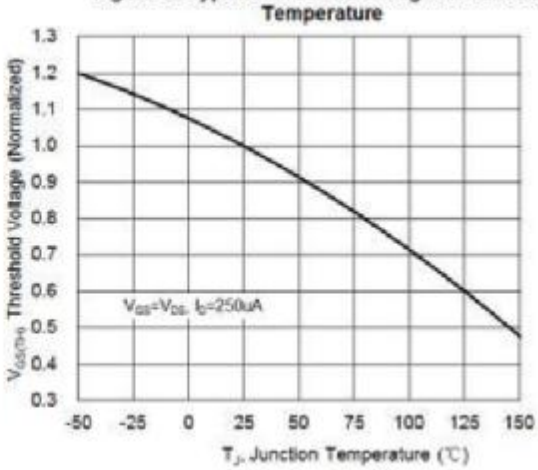


Figure 13. Maximum Forward Safe Operation Area

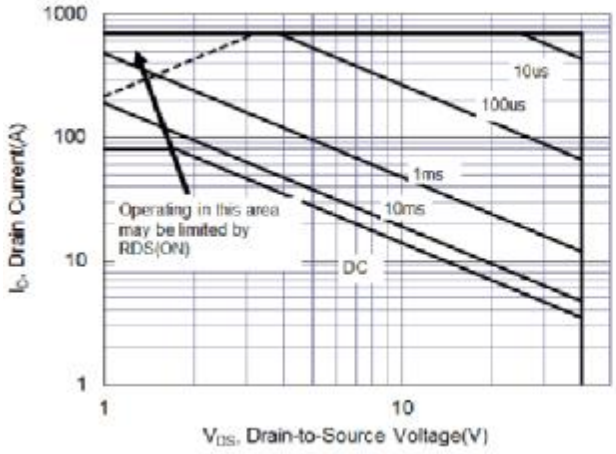


Figure 14. Typical Capacitance vs. Drain-to-Source Voltage

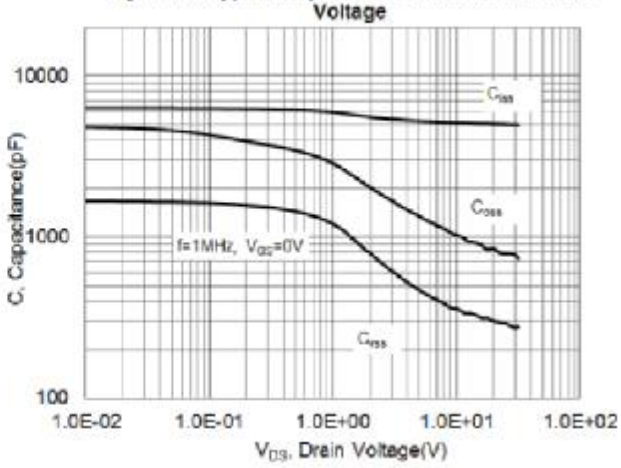


Figure 15. Typical Gate Charge vs. Gate-to-Source Voltage

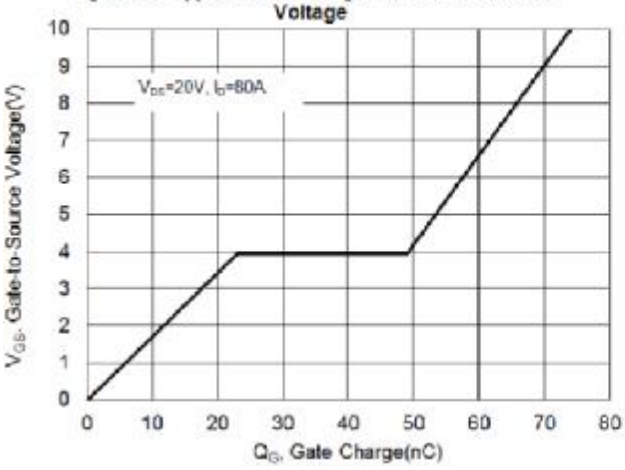
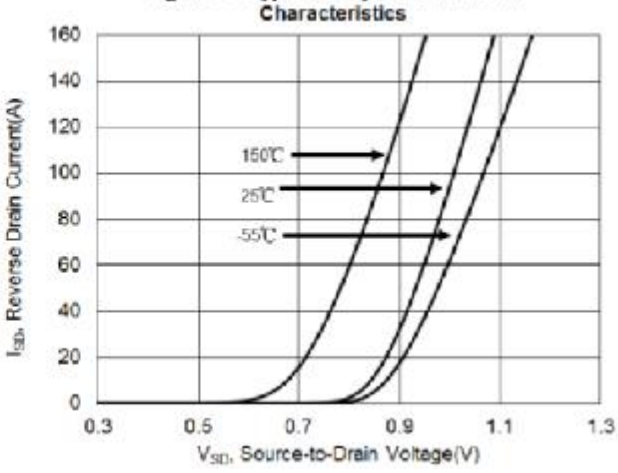


Figure 16. Typical Body Diode Transfer Characteristics



9. Test Circuits and Waveforms

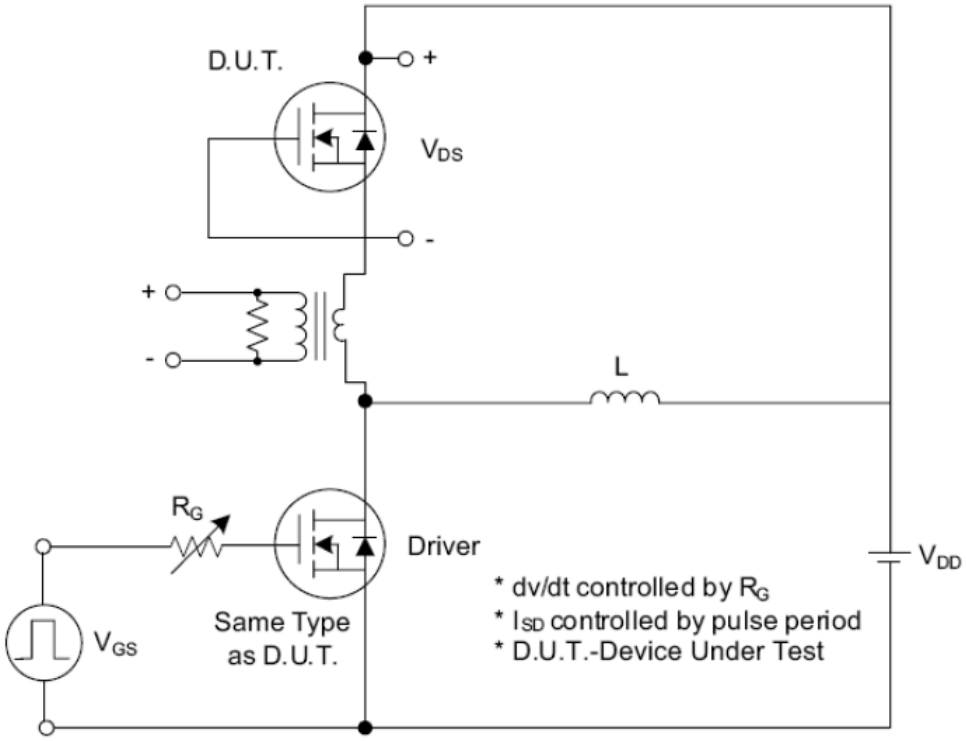


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

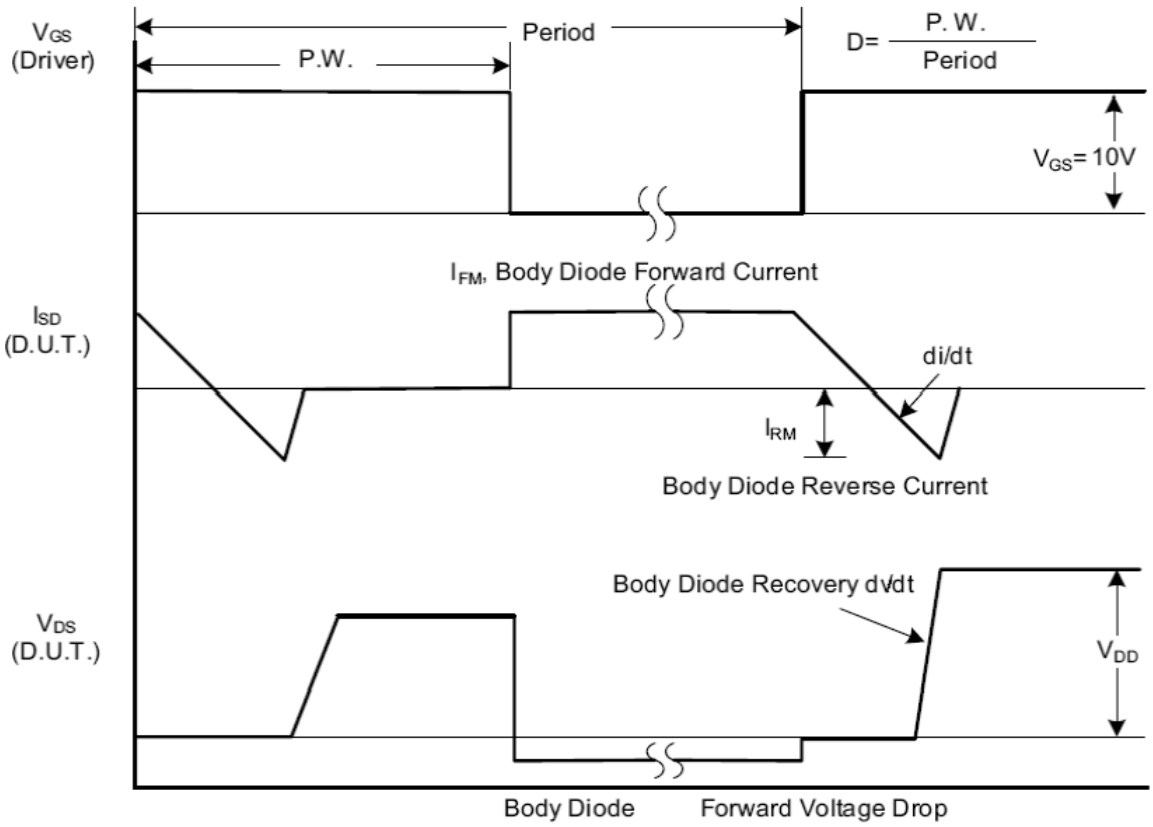


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

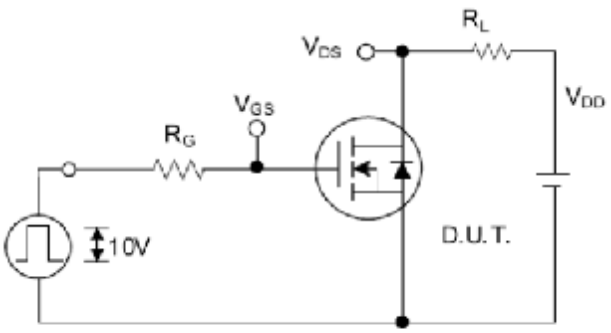


Fig. 2.1 Switching Test Circuit

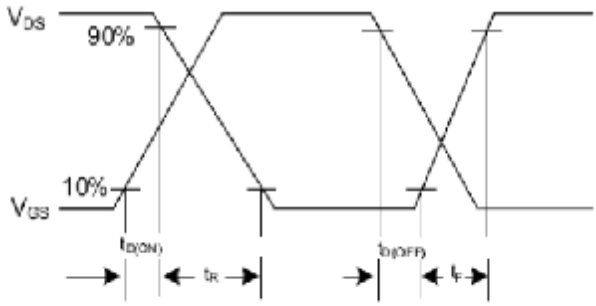


Fig. 2.2 Switching Waveforms

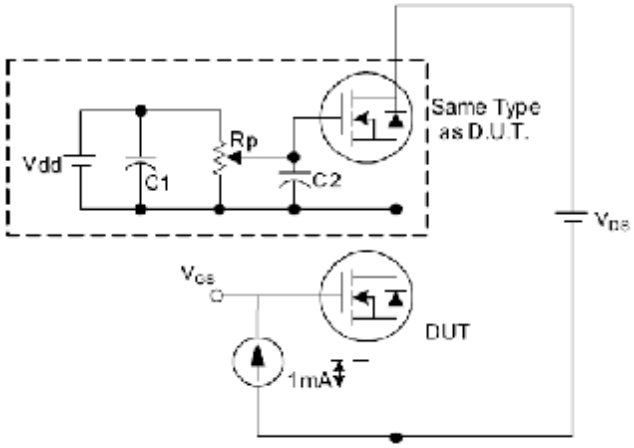


Fig. 3 . 1 Gate Charge Test Circuit

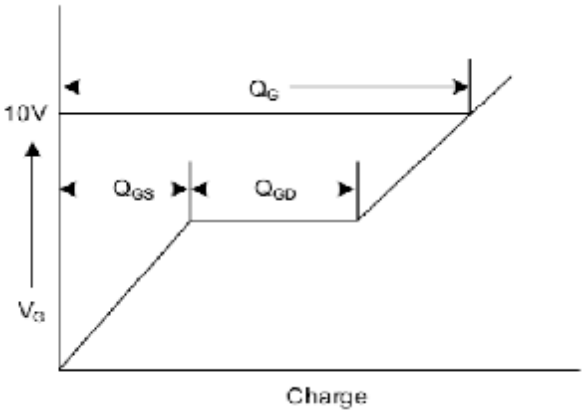


Fig. 3 . 2 Gate Charge Waveform

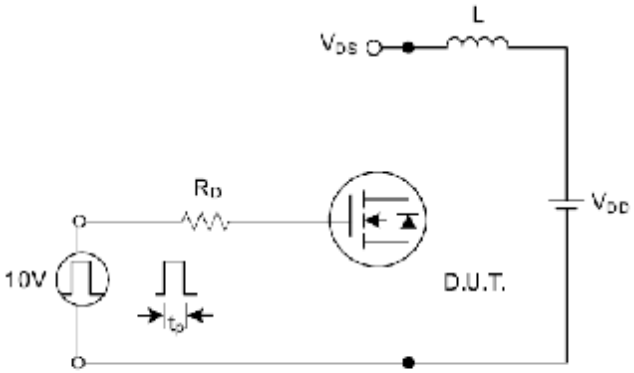


Fig. 4.1 Unclamped Inductive Switching Test Circuit

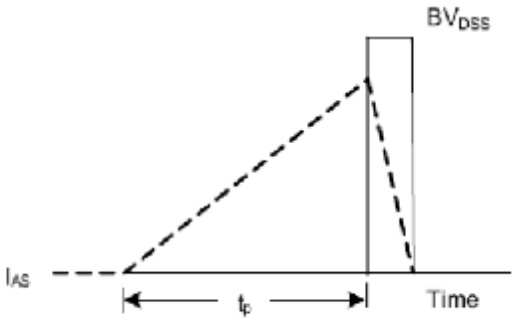


Fig. 4.2 Unclamped Inductive Switching Waveforms